Listing of Claims

1. (Currently Amended) A circuit ~~board~~, comprising:

a detector ~~transmitter~~ to detect loss in a link coupled to a transmitter; [[and]]

a controller ~~an equalizer~~ to automatically determine a multi-tap equalization setting based on the loss detected in the ~~of a~~ link coupled to the transmitter; and

an equalizer to generate a pulse signal to equalize transmission of data on the link based on the multi-tap equalization setting, the pulse signal having a plurality of levels that respectively correspond to at least one pre-cursor and at least one post-cursor of a main pulse, the transmission of said data to be equalized based on the at least one pre-cursor and at least one post-cursor.

2. (Currently Amended) The circuit ~~board~~ of claim 1, wherein the equalization setting is a two-tap equalization setting.

3. (Currently Amended) The circuit ~~board~~ of claim 1, wherein the equalization setting is a five-tap equalization setting.

4. (Currently Amended) The circuit ~~board~~ of claim 1, wherein the detector is to detect loss in the link based on ~~further comprising: receiving~~ a signal which includes link loss information received through a predetermined channel.

5. (Currently Amended) The circuit ~~board~~ of claim 1, further comprising:

a look-up table to store a plurality of predetermined tap coefficient settings that correspond to ~~settings in correspondence with~~ a respective number of link loss values,

~~the equalizer searching~~ the control circuit to search the look-up table for a tap coefficient setting that corresponds to ~~setting which corresponds to~~ the detected link loss, the levels in the pulse signal respectively corresponding to tap coefficients included in the setting produced by the search.

6. (Currently Amended) The circuit ~~board~~ of claim 1, wherein the controller ~~equalizer~~ determines the equalization setting during link initialization.

7. (Currently Amended) The circuit ~~board~~ of claim 1, wherein at least one of the equalizer or the controller receives information indicative of voltage and timing margins of an eye diagram at a receiver and adjusts the equalization setting based on the voltage and timing margins.

8. (Currently Amended) A method, comprising:

measuring loss in a link between a transmitter and a receiver; [[and]]

automatically determining a multi-tap equalization setting for the transmitter based on the measured loss; and

generating a pulse signal to equalize transmission of data on the link based on the multi-tap equalization setting, the pulse signal having a plurality of levels that respectively correspond to at least one pre-cursor and at least one post-cursor of a main pulse, the transmission of said data to be equalized based on the at least one pre-cursor and at least one post-cursor.

9. (Original) The method of claim 8, wherein the equalization setting is a two-tap coefficient setting.

10. (Original) The method of claim 9, wherein the equalization setting is a five-tap coefficient setting.

11. (Original) The method of claim 8, wherein measuring the loss is performed at the receiver.

12. (Original) The method of claim 11, wherein measuring the loss includes:

transmitting a clock signal from the transmitter to the receiver; and

computing the loss as a ratio of the transmitted clock signal amplitude and the received clock signal amplitude.

13. (Original) The method of claim 12, wherein the receiver receives the clock signal through an input which is offset calibrated.

14. (Original) The method of claim 13, wherein the receiver sweeps the offset to determine the amplitude of the received clock signal to within a predetermined error.

15. (Original) The method of claim 14, wherein the predetermined error is one LSB error.

16. (Original) The method of claim 14, wherein the loss is measured based on the following equation:

$$\text{Loss (dB)} = -20 \log (N_{AC}/N_{DC})*(Vdc\_eq/V_{swing})$$

where N_{AC} is a number of steps to determine the amplitude of the received clock signal, N_{DC} is a number of steps to determine a voltage swing of a DC voltage transmitted to the receiver, Vdc_eq is an equalized DC voltage, and V_{swing} is the voltage swing.

17. (Currently Amended) The method of claim 8, further comprising:

storing a look-up table that includes a plurality of predetermined tap coefficient settings in correspondence with a respective number of loss values, wherein determining the equalization setting includes searching the look-up table for a tap coefficient setting which corresponds to the measured loss, the levels in the pulse signal respectively corresponding to ~~and setting an equalizer in the transmitter based on the~~ tap coefficient s ~~setting~~ included in the setting obtained from the search.

18. (Original) The method of claim 17, wherein measuring the loss and determining the multi-tap equalization setting are performed during link initialization.

19. (Original) The method of claim 8, further comprising:

measuring voltage and timing margins of an eye diagram at the receiver; and

tuning the multi-tap equalization setting based on the voltage and timing margins.

20. (Currently Amended) A system, comprising:

a first circuit;

a second circuit; and

a data link connecting the first and second circuits,

wherein at least one of the first or ~~and~~ second circuits includes:

(a) a detector ~~transmitter~~ to detect loss in a link coupled to a transmitter; [[and]]

(b) a controller ~~an equalizer~~ to automatically determine a multi-tap equalization setting based on ~~a measured~~ the loss detected in the data ~~of the~~ link; and

(c) an equalizer to generate a pulse signal to equalize transmission of data on the link based on the multi-tap equalization setting, the pulse signal having a plurality of levels that respectively correspond to at least one pre-cursor and at least one post-cursor of a main pulse, the transmission of said data to be equalized based on the at least one pre-cursor and at least one post-cursor.

21. (Original) The system of claim 20, wherein the first circuit includes a chipset and the second circuit includes a CPU.

22. (Original) The system of claim 20, wherein the first circuit includes a chipset and the second circuit includes a memory.

23. (Original) The system of claim 20, wherein the memory is one of a RAM and a cache.

24. (Original) The system of claim 20, wherein the first circuit includes a memory and the second circuit includes a CPU.

25. (Original) The system of claim 20, wherein the first circuit includes a graphical interface and the second circuit includes at least one of a memory, CPU, and chipset.

26. (Currently Amended) The system of claim 20, wherein said at least one of the first or ~~and~~ second circuits include:

a look-up table to store a plurality of predetermined tap coefficient settings that correspond to ~~settings in correspondence with~~ a respective number of link loss values, ~~the equalizer searching~~ the control circuit to search the look-up table for a tap coefficient setting that corresponds to ~~setting which correspond to~~ the detected link loss, the levels in the pulse signal respectively corresponding to tap coefficients included in the setting produced by the search.

27. (Original) The system of claim 20, wherein the controller ~~equalizer~~ determines the equalization setting during link initialization.

28. (Currently Amended) A computer-readable medium storing a program to control equalization in a transmission circuit ~~board~~, said program including:

a first code section to search a look-up table based on loss of a link coupled to the transmission circuit ~~connected to the board~~, said table storing a plurality of tap coefficient settings in correspondence with a respective number of loss values; and

a second code section to adjust equalization of the transmission circuit ~~an equalizer~~ based on a tap coefficient setting generated from the search, the second code section adjusting the equalization by generating a pulse signal having a plurality of levels that respectively correspond to at least one pre-cursor and at least one post-cursor of a main pulse, the transmission of said data to be equalized based on the at least one pre-cursor and at least one post-cursor.

29. (Original) The computer-readable medium of claim 28, wherein the second code section adjusts the equalizer based on the tap coefficient setting during link initialization.

30. (Original) The computer-readable of claim 28, further comprising:

a third code section which tunes the equalization setting based on voltage and timing margins of a receiver eye diagram.

31. (New) The circuit of claim 1, wherein one or more levels of the pulse signal that correspond to the at least one pre-cursor have a first polarity and one or more levels of the pulse signal that correspond to the at least on post-cursor have a second polarity opposite to the first polarity.

32. (New) The circuit of claim 31, wherein the one or more levels of the pulse signal that having the second polarity substantially negate a first-polarity component of the main pulse.

33. (New) The circuit of claim 1, wherein one or more levels of the pulse signal that correspond to the at least one pre-cursor reduce rise-time delay in data transmission noise.

34. (New) The circuit of claim 1, wherein said data is to be transmitted between the transmitter and another circuit, the transmitter and other circuit residing on a same circuit board.